In the Claims

1. (Currently Amended) A unified memory architecture that decouples a color buffer from a main memory in a computer, the architecture comprising:

a sole memory controller connected to the main memory to manage use of the main memory between a graphics subsystem and a processing unit, the memory controller operable for partitioning an address space for the color buffer in main memory into two logical buffers, operable for designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory, operable for connecting the frame-preparation memory to the graphics subsystem and operable for connecting the refresh memory to a display device, wherein color data is written into the frame-preparation memory at a frame rate, ~~and~~ read from the refresh memory at a rate that supports a refresh rate of the display device and the graphics subsystem includes a 2D graphics engine.

2. (Currently Amended) ~~The unified memory architecture of claim 1~~A unified memory architecture that decouples a color buffer from a main memory in a computer, the architecture comprising:

a sole memory controller connected to the main memory to manage use of the main memory between a graphics subsystem and a processing unit, the memory controller operable for partitioning an address space for the color buffer in main memory into two logical buffers, operable for designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory, operable for connecting the frame-preparation memory to the graphics subsystem and operable for connecting the refresh memory to a display device, wherein color data is written into the frame-preparation memory at a frame rate, read from the refresh memory at a rate that supports a refresh rate of the display device, and ~~wherein~~ the address space for the refresh memory is mapped

into a physical memory device for a dedicated memory that is separate from a physical memory device for the main memory.

3. (Previously Presented) The unified memory architecture of claim 1, wherein the memory controller is further operable for copying the color data from the frame-preparation memory to the refresh memory.

4. (Previously Presented) The unified memory architecture of claim 3, wherein the memory controller copies the color data at pre-determined intervals.

5. (Previously Presented) The unified memory architecture of claim 3, wherein the memory controller copies the color data when an entire frame of color data is ready for display.

6. (Previously Presented) The unified memory architecture of claim 1, wherein the memory controller is further operable for further partitioning the address space for the color buffer into a third logical buffer, for designating the third logical buffer as a transfer memory, and for copying the color data from the transfer memory to the refresh memory.

7. (Previously Presented) The unified memory architecture of claim 6, wherein the memory controller is further operable for disconnecting the logical buffer currently designated as the frame-preparation memory from the graphics subsystem, and connecting the logical buffer currently designated as the transfer memory to the graphics subsystem to switch the designations of the logical buffers.

8. (Previously Presented) The unified memory architecture of claim 7, wherein the memory controller switches the designations of the logical buffers when an entire frame

of color data is ready for display in the logical buffer currently designated as the frame-preparation memory.

9. (Previously Presented) The unified memory architecture of claim 1, wherein the memory controller is operable for connecting the logical buffer currently designated as the frame-preparation memory to the display device and the logical buffer currently designated as the refresh memory to the graphics subsystem to switch the designations of the logical buffers.

10. (Currently Amended) A method of decoupling a color buffer from a main memory by a sole memory controller in a computer having a unified memory architecture, the memory controller managing use of the main memory between a graphics subsystem and a processing unit, wherein the graphics subsystem includes a 2D graphics engine, the method comprising:

partitioning an address space for the color buffer in the main memory into first and second logical buffers;

designating the first logical buffer as a refresh memory and designating the second logical buffer as a frame-preparation memory;

writing color data into the frame-preparation memory at a frame rate;

copying the color data from the frame-preparation memory to the refresh memory; and

reading the color data from the refresh memory at a rate that supports a refresh rate of a display device.

11. (Currently Amended) ~~The method of claim 10, further comprising~~ A method of decoupling a color buffer from a main memory by a sole memory controller in a computer

having a unified memory architecture, the memory controller managing use of the main memory between a graphics subsystem and a processing unit, the method comprising:

partitioning an address space for the color buffer in the main memory into first and second logical buffers;

designating the first logical buffer as a refresh memory and designating the second logical buffer as a frame-preparation memory;

writing color data into the frame-preparation memory at a frame rate;

copying the color data from the frame-preparation memory to the refresh memory;

reading the color data from the refresh memory at a rate that supports a refresh rate of a display device, and;

mapping the address space for the refresh memory onto a physical memory device for a dedicated memory separate from a physical memory device for the main memory.

12. (Previously Presented) The method of claim 10, wherein the color data is copied from the frame-preparation memory to the refresh memory when an entire frame of color data is ready for display.

13. (Previously Presented) The method of claim 10, wherein the color data is copied from the frame-preparation memory to the refresh memory at pre-determined intervals.

14. (Previously Presented) The method of claim 10, further comprising:

further partitioning the address space of the color buffer into a third buffer;

designating the third buffer as a transfer memory;

building a first frame of color data in the frame-preparation memory;

switching the designation of the second buffer with the designation of the third buffer when the first frame of color data is ready for display;

building a second frame of color data in the frame-preparation memory; and

switching the designation of the third buffer with the designation of the second buffer when the second frame of color data is ready for display,

wherein copying the color data from the frame-preparation memory to the refresh memory is accomplished by copying the color data from the buffer currently designated as the transfer memory.

15. (Currently Amended) A computer system having a unified memory architecture, the computer system comprising:

a processing unit;

a main memory connected to the processing unit though a system bus, the main memory being partitioned into an address space for a color buffer;

a sole memory controller connected to the main memory to manage use of the main memory between a graphics subsystem and the processing unit;

a graphics subsystem connected to the main memory through the memory controller to create a frame of color data in the color buffer at a frame rate, wherein the graphics subsystem includes a 2D graphics engine; and

a display device connected to the main memory through the memory controller, to display a frame of color data from the color buffer at a refresh rate,

wherein the memory controller decouples the color buffer from the main memory by:

partitioning the address space for the color buffer in main memory into two logical buffers;

designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory;

connecting the frame-preparation memory to the graphics subsystem;

connecting the refresh memory to the display device; and

copying the color data from the frame-preparation memory to the refresh memory.

16. (Currently Amended) ~~The computer system of claim 15, further comprising~~ A computer system having a unified memory architecture, the computer system comprising:

a processing unit;

a main memory connected to the processing unit though a system bus, the main memory being partitioned into an address space for a color buffer;

a sole memory controller connected to the main memory to manage use of the main memory between a graphics subsystem and the processing unit;

a graphics subsystem connected to the main memory through the memory controller to create a frame of color data in the color buffer at a frame rate; and

a display device connected to the main memory through the memory controller, to display a frame of color data from the color buffer at a refresh rate,

wherein the memory controller decouples the color buffer from the main memory by:

partitioning the address space for the color buffer in main memory into two logical buffers;

designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory;

connecting the frame-preparation memory to the graphics subsystem;

connecting the refresh memory to the display device;

copying the color data from the frame-preparation memory to the refresh memory; and

a memory device for a dedicated memory separate from a memory device for the main memory and the memory controller further maps the address space for the refresh memory to the memory device for the dedicated memory.

17. (Previously Presented) The computer system of claim 15, wherein the memory controller copies the color data at pre-determined intervals.

18. (Previously Presented) The computer system of claim 15, wherein the memory controller copies the color data when an entire frame of color data is ready for display.

19. (Previously Presented) The computer system of claim 15, wherein the memory controller further partitions the address space for the color buffer into a third logical buffer, designates the third logical buffer as a transfer memory and copies the color data from the transfer memory to the refresh memory in lieu of copying the color data from the frame-preparation memory.

20. (Previously Presented) The computer system of claim 19, wherein the memory controller further switches the designations of the logical buffers by connecting the logical buffer currently designated as the frame-preparation memory to the display system and by connecting the logical buffer currently designated as the transfer memory to the graphics subsystem.

21. (Previously Presented) The computer system of claim 20, wherein the memory controller switches the designations of the logical buffers when an entire frame of color data is ready for display in the logical buffer currently designated as the frame-preparation memory.

22. (Currently Amended) An apparatus for use in a unified memory architecture comprising:

means for preparing color data for display; and

a sole means for controlling use of a main memory between the means for preparing and a processing unit, for partitioning an address space in the main memory that represents a color buffer into first and second logical buffers, for designating the first logical buffer as a refresh memory and the second logical buffer as a frame-preparation

memory, for writing the color data into the frame-preparation memory at a frame rate, for copying the color data from the frame-preparation memory to the refresh memory, and for reading the color data from the refresh memory at a rate that supports a refresh rate of a display device, wherein the graphics subsystem includes a 2D graphics engine.

23. (Currently Amended) ~~The apparatus of claim 22~~ An apparatus for use in a unified memory architecture comprising:

means for preparing color data for display; and

a sole means for controlling use of a main memory between the means for preparing and a processing unit, for partitioning an address space in the main memory that represents a color buffer into first and second logical buffers, for designating the first logical buffer as a refresh memory and the second logical buffer as a frame-preparation memory, for writing the color data into the frame-preparation memory at a frame rate, for copying the color data from the frame-preparation memory to the refresh memory, and for reading the color data from the refresh memory at a rate that supports a refresh rate of a display device, wherein the means for controlling further maps the address space for the refresh memory onto a physical memory device for a dedicated memory separate from a physical memory device for the main memory.

24. (Previously Presented) The apparatus of claim 22, wherein the means for controlling copies the color data from the frame-preparation memory to the refresh memory when an entire frame of color data is ready for display.

25. (Previously Presented) The apparatus of claim 22, wherein the means for controlling copies the color data from the frame-preparation memory to the refresh memory at pre-determined intervals.

26. (Previously Presented) The apparatus of claim 22, wherein the means for controlling is further operable for partitioning the address space of the color buffer into a third buffer, designating the third buffer as a transfer memory, building a first frame of color data in the frame-preparation memory, switching the designation of the second buffer with the designation of the third buffer when the first frame of color data is ready for display, building a second frame of color data in the frame-preparation memory, and switching the designation of the third buffer with the designation of the second buffer when the second frame of color data is ready for display, and wherein the means for controlling copies the color data from the frame-preparation memory to the refresh memory by copying the color data from the buffer currently designated as the transfer memory.